

What is claimed is:

1. An impedance standard substrate for calibrating a vector network analyzer comprising:

a first surface;

a second surface opposite to the first surface; and

6 a thru-circuit having two contacts electrically connected to each other and respectively disposed on the first surface and the second surface.

2. The impedance standard substrate as claimed in claim 1, wherein the substrate comprises a via electrically connected to the two contacts.

3. The impedance standard substrate as claimed in claim 2, wherein the two contacts are disposed by the opposite sides of the via, respectively.

12 4. The impedance standard substrate as claimed in claim 2, wherein the two contacts are disposed by the same side of the via.

5. The impedance standard substrate as claimed in claim 1, further comprising a side wall defined between the first surface and the second surface, wherein the two contacts of the thru-circuit abut the edge of the impedance standard substrate and the thru-circuit further comprises a trace disposed on the side wall for electrically
18 connecting the two contacts.

6. The impedance standard substrate as claimed in claim 5, wherein the trace is disposed by circuit layout on the side wall.

7. The impedance standard substrate as claimed in claim 1, further comprising a pair of open-circuits disposed on the first surface and the second surface, respectively.

24 8. The impedance standard substrate as claimed in claim 1, further comprising a pair of short-circuits disposed on the first surface and the second surface, respectively.

9. The impedance standard substrate as claimed in claim 1, further comprising a pair of load-circuits disposed on the first surface and the second surface, respectively.

10. A method for calibrating a vector network analyzer, which generates a measuring signal and comprises two probes for transmitting the measuring signal, comprising the steps of:

providing an impedance standard substrate which has a first surface and a second surface opposite to the first surface;

providing a thru-circuit having two contacts electrically connected to each other and respectively disposed on the first surface and the second surface; and

6 driving the two probes to be in contact with the two contacts, respectively, and sending the measuring signal.

11. The method as claimed in claim 10, further comprising the steps of:

providing a pair of open-circuits disposed on the first surface and the second surface, respectively; and

driving the two probes to be in contact with the open-circuits, respectively, and sending the measuring signal.

12 12. The method as claimed in claim 10, further comprising the steps of:

providing a pair of short-circuits disposed on the first surface and the second surface, respectively; and

driving the two probes to be in contact with the short-circuits, respectively, and sending the measuring signal.

13. The method as claimed in claim 10, further comprising the steps of:

18 providing a pair of load-circuits disposed on the first surface and the second surface, respectively; and

driving the two probes to be in contact with the load-circuits, respectively, and sending the measuring signal.

14. The method as claimed in claim 10, wherein the thru-circuit comprises a via electrically connected to the two contacts.

24 15. The method as claimed in claim 10, wherein the impedance standard substrate further comprises a side wall between the first surface and the second surface, the contacts of the thru-circuit abut the edge of the impedance standard substrate, and the thru-circuit further comprises a trace disposed on the side wall for electrically connecting the two contacts.

16. An impedance standard substrate for calibrating a vector network analyzer comprising:

a copper core defining a first surface and a second surface;

a first isolation layer covering the first surface of the copper core;

a second isolation layer covering the second surface of the copper core; and

6 a thru-circuit having two contacts respectively disposed on the first isolation layer and the second isolation layer, and electrically connected to the copper core.

17. The impedance standard substrate as claimed in claim 16, further comprising a pair of open-circuits disposed on the first isolation layer and the second isolation layer, respectively.

12 18. The impedance standard substrate as claimed in claim 16, further comprising a pair of short-circuits disposed on the first isolation layer and the second isolation layer, respectively.

19. The impedance standard substrate as claimed in claim 16, further comprising a pair of load-circuits disposed on the first isolation layer and the second isolation layer, respectively.

18 20. The impedance standard substrate as claimed in claim 16, wherein the first and the second isolation layers are made of BT resin (Bismaleimide Triazine resin).

21. The impedance standard substrate as claimed in claim 16, wherein each of the first and the second isolation layers comprises a through hole for defining the contacts of the thru-circuit.